1   1.   A method comprising:

2   storing data at a first density in a first cell

3 in a first memory; and

4   storing data at a second density in a second cell

5 in the first memory.

1   2.   The method of claim 1 wherein storing data at a

2 second density in a second cell includes storing fewer bits

3 per cell in one of said first or second cells.

1   3.   The method of claim 1 including changing the

2 number of bits stored per cell on the fly.

1   4.   The method of claim 2 including storing data at

2 levels which are spaced from one another in said cell in

3 order to improve the read fidelity.

1   5.   The method of claim 4 including storing data in a

2 cell including a plurality of levels and filling less than

3 all of said levels.

1   6.   The method of claim 5 including storing data in

2 regularly spaced levels within a cell while leaving

3 intervening levels within the cell unoccupied by stored

4 data.

1   7.   An article comprising a medium storing
2 instructions that enable a processor-based system to:
3   store data at a first density in a first cell in
4 a first memory; and
5   store data at a second density in a second cell
6 in said first memory.

1   8.   The article of claim 7 further storing
2 instructions that enable the processor-based system to
3 store fewer bits per cell in one of said first or second
4 cells.

1   9.   The article of claim 7 further storing
2 instructions that enable the processor-based system to
3 change the number of bits stored per cell on the fly.

1   10.   The article of claim 8 further storing
2 instructions that enable the processor-based system to
3 store data at levels which are spaced from one another in
4 said cell in order to improve the read fidelity.

1   11.   The article of claim 10 further storing
2 instructions that enable the processor-based system to
3 store data in a cell including a plurality of levels and
4 fill less than all of said levels.

1   12. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 store data in regularly spaced levels within a cell while
4 leaving intervening levels within the cell unoccupied by
5 stored data.

1   13. A memory comprising:
2   a memory array including a first and second cell;
3 and
4   a controller coupled to said array to store data
5 in said array at a first density in the first cell and to
6 store data at a second density in the second cell.

1   14. The memory of claim 13 wherein said memory is a
2 flash memory.

1   15. The memory of claim 14 wherein said memory is a
2 multi-level cell memory.

1   16. The memory of claim 13 wherein said controller
2 stores fewer bits per cell in one of said first or second
3 cells.

1   17. The system of claim 13 wherein said controller
2 changes the number of bits stored per cell on the fly.

1   18. The memory of claim 17 wherein said controller
2 stores data at levels that are spaced from one another in
3 said cell in order to improve the read fidelity.

1   19. The memory of claim 18 wherein said controller
2 stores data in a cell including a plurality of levels and
3 fills less than all of the levels.

1   20. The memory of claim 13 wherein said controller
2 stores data in regularly spaced levels within a cell while
3 leaving intervening levels within the cell unoccupied by
4 stored data.